Design a NMOS and PMOS transistor circuit using virtuoso cadence and plot I-V characteristics of PMOS and NMOS for different gate and drain voltages

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***Abstract*—In this project we simulate NMOS and PMOS transistor circuit in cadence virtusso tool and the I/V characteristics of PMOS and NMOS are observed**

***Index Terms*—PMOS.NMOS,THRESOLD VOLTAGE,DRAIN CURRENT**

I. Introduction

A. NMOS:

A Metal-Oxide-Semiconductor Field-Effect Transistor(MOSFET) is a four terminal device whose terminals are named as Gate(G), Drain(D), Source(S) and Bulk(B).

A cross-sectional view of n-channel enhancement mode transistor is shown in Figure 1.

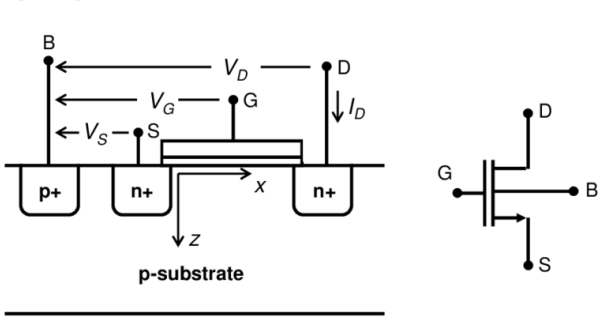

Fig. 1. NMOS

NMOS is symmetric four terminal device with P-substrate and n-type drain and source.The current flow between drain and souce when gate voltage is connected to Positive voltage The positive voltage attracts free-floating electrons within the body towards the gate, forming a conductive channel. But first, enough electrons must be attracted near the gate to counter the dopant ions added to the body of the FET; this forms a region free of mobile carriers called a depletion region, and the voltage at which this occurs is referred to as the threshold voltage of the FET. Further gate-to-source voltage increase will attract even more electrons towards the gate which are able to create a conductive channel from source to drain; this process is called inversion.

From square law model of an n-channel MOS transistor, drain to source current is given by

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B. PMOS:

PMOS (pMOSFET) is a type of MOSFET. A PMOS transistor is made up of p-type source and drain and a n-type substrate. When a positive voltage is applied between the source and the gate (negative voltage between gate and source), a p-type channel is formed between the source and the drain with opposite polarities. A current is carried by holes from source to the drain through an induced p-type channel. A high voltage on the gate will cause a PMOS not to conduct, while a low voltage on the gate will cause it to conduct. Logic gates and other digital devices implemented using PMOS are said have PMOS logic. PMOS technology is low cost and has a good noise immunity

A cross-sectional view of p-channel enhancement mode transistor is shown in Figure 2.

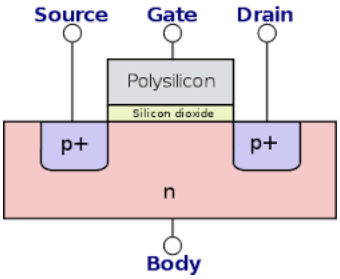

Fig. 2. PMOS

II. PMOS and NMOS schematics in cadence

A. NMOS schematic:

below figure consists of NMOS schematic in cadence virtuso tool

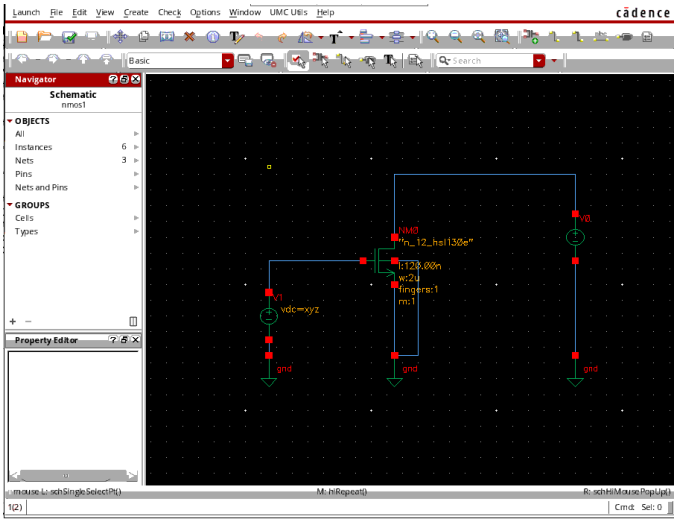

Fig. 3. NMOS schematic in cadence virtuoso

B. PMOS schematic

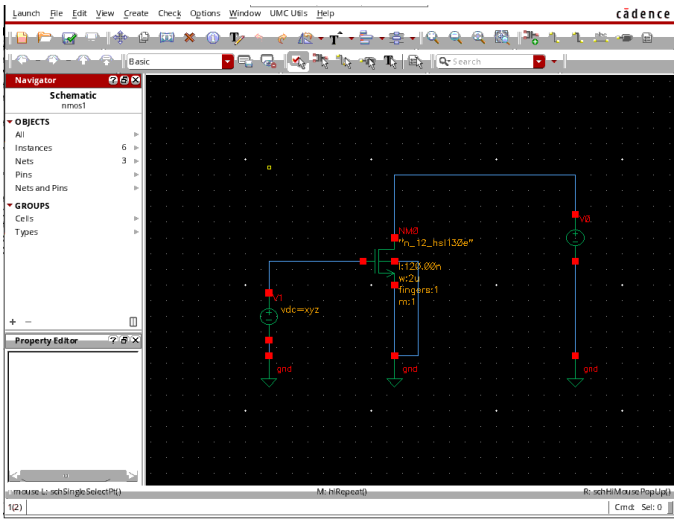

Fig. 4. NMOS schematic in cadence virtuoso

III. $I-V$ CHARCETERISTICS OF NMOS AND PMOS

A. *MOSFET output characteristics plot ID versus VDS for several values of VGS.*

The characteristics of an nMOS transistor can be explained as follows. As the voltage at the gate increases further, electrons are attracted to the surface. At a particular voltage level, the electron density at the surface exceeds the hole density,this voltage leval is called thresold voltage. At this voltage, the surface has inverted from the p-type polarity of the substrate to an n-type inversion layer, or inversion region, directly underneath the gate. This inversion region is an extremely shallow layer, existing as a charge sheet directly below the gate. In the MOS capacitor, the high density of electrons in the inversion layer is supplied by the electronhole

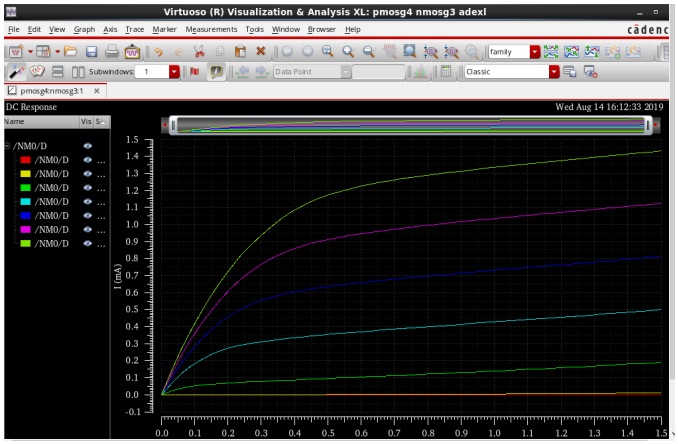

Fig. 5. NMOS I-V curve when gate volate is varying in cadence virtuoso

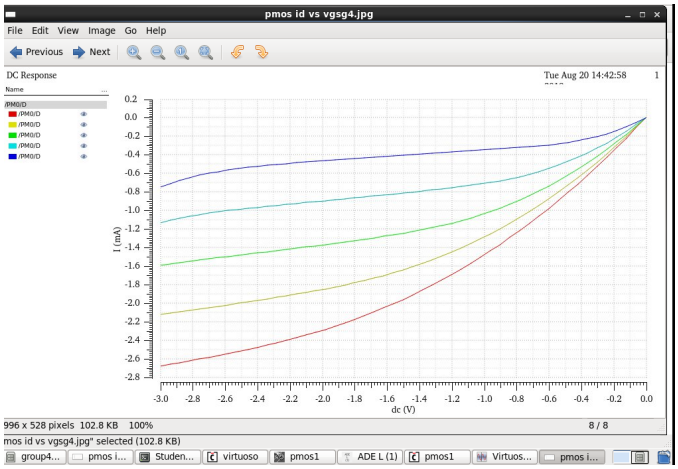

Fig. 6. PMOS I-V curve when gate voltage is varying in cadence virtuoso

generation process within the depletion layer. The positive charge on the gate is balanced by the combination of negative charge in the inversion layer plus negative ionic acceptor charge in the depletion layer. The voltage at which the surface inversion layer just forms plays an extremely important role in field-effect transistors and is called the threshold voltage V_{tn}. The region of output characteristics where V_{GStn} and no current flows is called the cutt-off region. When the channel forms in the nMOS (pMOS) transistor, a positive (negative) drain voltage with respect to the source creates a horizontal electric field moving the electrons (holes) toward the drain forming a positive (negative) drain current coming into the transistor. The positive current convention is used for electron and hole current, but in both cases electrons are the actual charge carriers. If the channel horizontal electric field is of the same order or smaller than the vertical thin oxide field, then the inversion channel remains almost uniform along the device length. This continuous carrier profile from drain to source puts the transistor in a bias state that is equivalently called either the non-saturated, linear, or ohmic bias state. The drain and source are effectively short-circuited. This happens

when VGS ¿ VDS + Vtn for nMOS transistor and VGS ¡ VDS +Vtp for pMOS transistor. Drain current is linearly related to drain-source voltage over small intervals in the linear bias state.

But if the nMOS drain voltage increases beyond the limit, so that VGS ¡ VDS + Vtn, then the horizontal electric field becomes stronger than the vertical field at the drain end, creating an asymmetry of the channel carrier inversion distribution shown in Figure 4

B. Transfer Characteristics

The transfer characteristic relates drain current (I_D) response to the input gate-source driving voltage (V_{GS}). Since the gate terminal is electrically isolated from the remaining terminals (drain, source, and bulk), the gate current is essentially zero, so that gate current is not part of device characteristics. The transfer characteristic curve can locate the gate voltage at which the transistor passes current and leaves the OFF-state. This is the device threshold voltage (Vtn). Figure 5 shows measured input characteristics for an nMOS and pMOS transistor with a small 0.1V potential across their drain to source terminals.

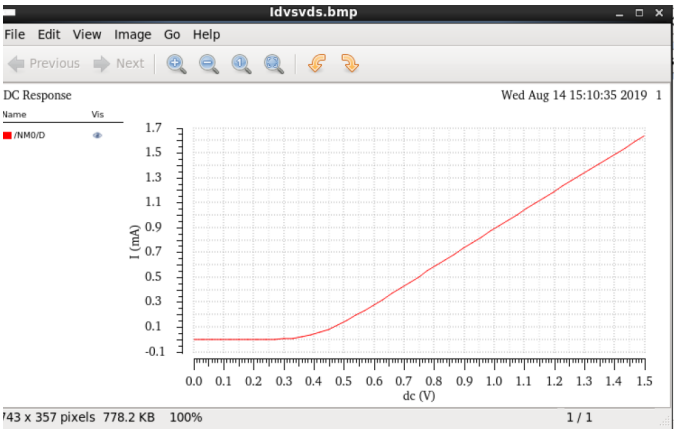

Fig. 7. NMOS I-V curve when drain volate is constant in cadence virtuoso

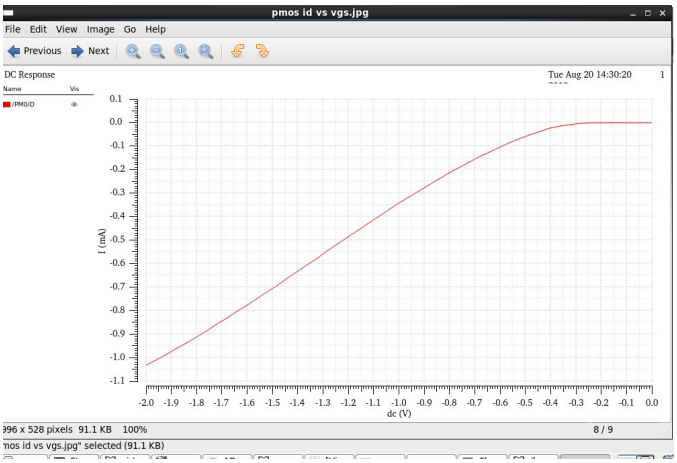

Fig. 8. PMOS I-V curve when drain voltage is constant in cadence virtuoso

The transistors are in their non-saturated bias states. As VGS increases for the nMOS transistor in Figure 5a, the threshold voltage is reached where drain current elevates. For VGS between 0V and 0.7V, ID is nearly zero indicating that the equivalent resistance between the drain and source terminals is extremely high. Once VGS reaches 0.7V, the current increases rapidly with VGS indicating that the equivalent resistance at the drain decreases with increasing gate-source voltage. Therefore, the threshold voltage of the given nMOS transistor is about Vtn 0.7V. The pMOS transistor input characteristic in Figure 5b is analogous to the nMOS transistor except the ID and VGS polarities are reversed.

C. Equations

1) NMOS: The current equation in cutoff($V_{GS} < V_{th}$ given by

$$I_D = 0 \tag{1}$$

The current equation in triode region given by

$$I_D = \mu_n C_{ox} W/L((V_{GS} - Vth)V_{DS} - 1/2V_{DS}^2) \tag{2}$$

The current equation in saturation region($V_{DS} > V_{GS} - V_{th}$) given by

$$I_D = 1/2\mu_n C_{ox} W/L(V_{GS} - Vth)^2 \tag{3}$$

subsubsectionPMOS

The current equation in cutoff($|V_{GS}| < V_{th}$ given by

$$I_D = 0 \tag{4}$$

The current equation in triode region given by

$$I_D = \mu_n C_{ox} W/L((V_{GS} - Vth)V_{DS} - 1/2V_{DS}^2) \tag{5}$$

The current equation in saturation region($V_{DS} > V_{GS} - V_{th}$) given by

$$I_D = 1/2\mu_n C_{ox} W/L(V_{GS} - Vth)^2 \tag{6}$$

IV. Conclusion:

- The schematic of NMOS and PMOS are designed in cadence tool successfully
- The I-V characteristics of PMOS and NMOS are successfully simulated and graphs are plotted

V. References

[1] S. M. Sze. Physics of Semiconductor Devices. John Wiley , Sons, Inc., New York, 1981